WE CLAIM:

1. An instruction segment storing method, comprising:

building an instruction segment,

determining whether the instruction segment satisfies a filtering condition, and

if the instruction segment satisfies the filtering condition, storing the instruction segment in a segment cache.

2. The method of claim 1, wherein the filtering condition may be met only if all instructions in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

3. The method of claim 1, wherein the filtering condition may be met only if at least one instruction in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

4. The method of claim 1, wherein the filtering condition may be met only if a predetermined number of instructions in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

5. The method of claim 1, wherein the filtering condition may be met only if an instruction of the segment by which the segment is to be indexed was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

6. An instruction segment storing method, comprising:

building an instruction segment,

determining, from location flags associated with instruction in the instruction segment, whether the instruction segment satisfies a filtering condition, and

if so, storing the instruction segment in a segment cache.

7. The method of claim 6, wherein the filtering condition may be met only if all instructions in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

8. The method of claim 6, wherein the filtering condition may be met only if at least one instruction in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

9. The method of claim 6, wherein the filtering condition may be met only if a predetermined number of instructions in the instruction segment assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

10. The method of claim 6, wherein the filtering condition may be met only if an instruction of the segment by which the segment is to be indexed was assembled into the instruction segment from an instruction cache of a front-end processing system in a processor.

11. A front end system for a processing agent, comprising:
an instruction cache system, and
an instruction segment system, comprising:
a segment cache, and
a segment builder provided in communication with the instruction cache system, to store a new instruction segment in the segment cache when a filtering condition is met.

12. The front end system of claim 11, further comprising a history map provided in communication with the segment builder to identify when the filtering condition is met.

13. The front end system of claim 12, wherein the history map is a direct mapped cache.

14. The front end system of claim 12, wherein the history map is a set associative cache.

15. The front end system of claim 14, wherein the history map comprises a plurality of cache entries having a width corresponding to a width of a tag address of an instruction pointer in the system.

16. The front end system of claim 14, wherein the history map comprises a plurality of cache entries having a width corresponding to a width of a portion of a tag address of an instruction pointer in the system.

17. The front end system of claim 11, wherein the instruction cache system outputs instructions and location flags to the segment builder, the segment builder determining whether